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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, February 2015
(2008 Scheme)
08.402 : DIGITAL ELECTRONICS AND LOGIC DESIGN (E)
(Special Supplementary)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** question. **Each** question carries **4** marks.

1. Compare TTL and CMOS logic families.
2. Draw the truth table and circuit of a full subtractor.
3. Define :
   1) propagation delay
   2) noise margin
4. Convert $(539.78)_{10}$ to (a) BCD code (b) XS – 3 code.
5. Explain how race-around condition is eliminated in J-K flipflop.
6. What are alphanumeric codes ? Explain any one alphanumeric code.
7. Implement the POS function expressed by π 1, 2, 5 by a suitable multiplexer.
8. Distinguish between PLA and PAL devices.
9. Mention the applications of 555 timer.
10. Explain the significance and application of gray code.

PART – B

Answer **any one** question from **each** Module. **Each** question carries **20** marks.

Module – I

11. a) Convert the following.
    i) $(1011.101)_2$ to decimal
    ii) $(AEOF)_{16}$ to octal
    iii) $(5235)_{10}$ to hexadecimal
    iv) Octal 67.25 to binary. **10**

    b) What are the different methods of representing negative numbers ? Give examples. **10**

P.T.O.

12. a) Prove the following :

    a) $AC + B\overline{C} + AB = AC + B\overline{C}$

    b) $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}\,C + AB\overline{C} = \overline{A}\,\overline{B} + B\overline{C}$ 10

    b) Find the minimal SOP expression for the function

    $F(A, B, C, D) = \sum m(0, 1, 2, 7, 8, 9, 10, 13) + \sum d(5, 15)$. 10

Module – II

13. a) Design a BCD to 7-segment decoder (Design need to be shown for any four output segments). 10

    b) Draw and explain the working of 2-input CMOS NAND and NOR gates. 10

14. a) Convert the following flipflops : 10

    i) D to JK

    ii) JK to T

    b) Design a parity generator/checker and explain the working of the same. 10

Module – III

15. a) Design a mod-12 counter and give its truth table. 10

    b) Explain the operation of astable multivibrator using 555 timer IC. 10

16. a) Briefly explain the operation of a 3-bit universal shift register. 10

    b) Draw the circuit of a D flip-flop using NAND gates and explain its operation. 10